Tutorial 1

Problem 1
(homework)
Compute the minimal DNF or CNF for the following combinational logic:
(A, B, C, D shall be input signals, E, F shall be output signals)

Problem 2
(solved at the problem session)
Design a CMOS NOR gate.
   a) What is the truth table of the combinational logic?
   b) Design a circuit using p-switch and n-switch
   c) How could the layout in silicon look like?
Hint: Compare with the CMOS NAND gate and use de-Morgan’s Rules.

Problem 3
Design the following gates using only p-switch and n-switch
   a) NAND gate with 4 inputs (solved at the problem session)
   b) NOR gate with 4 inputs (solved at the problem session)
      (homework from here on...)
   c) For the following combinational logic: \( \neg (a \lor (b \land c \land d)) \)
   d) For the following combinational logic: \( \neg (a \land (b \lor c) \lor d \land e) \)
Hint: Note the precedence rules for Boolean operators (\( \neg \) before \( \land \) before \( \lor \))!

Problem 4
(solved at the problem session)
   a) How can the common logic functions AND, OR, XOR be implemented using inverter, AND and NOR?
   b) How can arbitrary logic expressions be represented just with NOR gates? (Hint: consider CNF and de-Morgan’s rules)

Problem 5
(homework)
   a) Implement the sum signal S of a half adder using NOR gates.
   b) Implement the carry signal C of a half adder using NAND gates.
   c) Implement a full adder using p-switch and n-switch (either draw a net list on paper, or implement using System-C)