Tutorial 5

Problem 1
Consider a cache memory with the following parameters:
- frame size: 16 words á 64 bits
- line size: 4096 lines
- address length: 32 bits
- associativity: direct mapped

a) How many bits are required to address one byte within a word?
b) How many bits are required to select a cache line?
c) How many bits need to be compared at tag comparison?

Problem 2
Determine the size and associativity of various caches of your computer. Write a suitable test program that exercises memory accesses in different patterns.

Problem 3
Let us illustrate the operation of a cache controller at a very simple example. In our example cache, there shall be 4 cache lines with contents of one byte each. The cache shall be fully (4-way set) associative.
The replacement strategy shall be LRU (least recently used). This means if space runs out, the cache line shall be evicted that has been used the least recently.

The client (CPU) now accesses the following addresses through the cache:
1 5 6 8 2 6 1 5 4

a) Determine the following for each clock cycle: contents of the memory, tag addresses, and recently-used state
b) Mark evictions from the cache