Modern Computer Architecture

Lecture 1
Technical Background
Outline – Lecture 1

• Introduction

• Silicon Technology
  – MOS FET: N-Switch and P-Switch
  – Logical Gates
  – Combinatorial Circuits
Semiconductors: Silicon

- most commonly: Si, but also GaAs, InP
- Symbol: Si, Atomic #14
- 2nd most abundant element (after oxygen), 27.7% mass of the earth crust,
  → sand, glass
- diamond lattice

isolator, conducts electricity when doped
Semiconductors: Doping

**n-type**
- Too many electrons in grid
- Travel faster

**p-type**
- Too few electrons in grid ("holes")
- Travel slower
Semiconductors: p-n junction

- p-n junction can be crossed by electric current only in one direction
- application: diode, LED

\[ \text{p-type} \quad \text{n-type} \]

**holes**

**electrons**

**isolator**

**charge**

**conducts**

**doesn’t conduct**
• transistors can act as a switch for currents
• bipolar transistors most commonly used in analog electronics
• disadvantage: requires current in steady state
  → high power consumption
MOSFET in action

- Source
- Gate
- Drain
- Depletion region
- Voltage charge
- Inversion layer
- P substrate
- N+
FET: N-Switch

Source  Gate  Drain

Channel

\[
\begin{array}{c|c|c|c}
G & S & D \\
0 & X & Z \\
1 & 0 & 0 \\
1 & 1 & H \\
\end{array}
\]

- Polysilicon
- Silicon
- Silicondioxide
- Metal
FET: P-Switch

- Source
- Gate
- Drain

- Channel

- Polysilicon
- Silicon
- Silicondioxide
- Metal

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CMOS Inverter

- Logical Notation: $y = \neg x$
- Circuit Notation: $y := \text{NOT } x$

- if $x=1$: n-switch open, p-switch closed
- if $x=0$: n-switch closed, p-switch open

<table>
<thead>
<tr>
<th>$x$</th>
<th>$y$</th>
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<tbody>
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- ANSI (U.S.):

- EIC (deutsch):

- DIN 40 700 (deutsch):
CMOS NAND Gate

- Logical Notation: \( z = \neg (x \land y) \)
- Circuit Notation: \( z := \text{NOT} (x \text{ AND } y) \)

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<tr>
<th>x</th>
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- ANSI (U.S.):
  - Table: \( x \land y \)
  - Circuit Diagram:

- EIC (deutsch):
  - Table: \( x \land y \)
  - Circuit Diagram:

- DIN 40 700 (deutsch):
  - Table: \( x \land y \)
  - Circuit Diagram:
Latchup

- p and n areas in CMOS form bipolar transistors
- in normal operation, these transistors are not conducting
- power surges or radiation can render these transistors in conducting state
- effect: short-circuit, heat may lead to destruction of the device
Photolithography / Epitaxy

- physical vapor deposition (PVD)
- chemical vapor deposition (CVD)
- electrochemical deposition (ECD)
- molecular beam epitaxy (MBE)
- atomic layer deposition (ALD)

• vapor-phase epitaxy (VPE)

expose
etch

glass
mask
acid
photoresist
new material
substrate
Miniaturization in Microelectronics

10 µm
10 µm (1971) e.g., Intel 8008
3 µm (1975) e.g., Intel 8088
1.5 µm (1982) e.g., Intel 80286
1 µm (1985) e.g., Intel 80386
800 nm (1989) e.g., P5 Pentium 60 MHz
600 nm (1994) e.g., Motorola PowerPC 601
350 nm (1995) e.g., Pentium II Klamath
250 nm (1998) e.g., AMD K6-2
180 nm (1999) e.g., Coppermine E
130 nm (2000) e.g., PowerPC 7447
90 nm (2002) e.g., VIA C7
65 nm (2006) e.g., Core Duo
45 nm (2008) e.g., Core 2 (Wolfdale)
32 nm (2010) e.g., Core i3 (Clarkp)
22 nm (2011) e.g., Xeon E3-123
16 nm (c.2013)
11 nm (c.2015)

Dr. Gordon Cichon
16.04.2015
Silicon Wafer
• At the bottom: MOS FETs from p- and n-doted silicon
• Short wires made from poly-silicon
• Several metal layers (up to 10) wires increase in width
Hardware Development

- Concept Engineering, Marketing
- Behavioral Modeling, Requirement Validation
- Architecture, Bit-Precise Modeling (e.g. in System-C)
- Testbench, Verification
- Silicon Frontend: RTL Modeling (e.g. Verilog, VHDL), clock-precise, Synthesis $\rightarrow$ netlist
- Silicon Backend: Place&Route, Timing-/Power-Analysis $\rightarrow$ geometry
- Tapeout $\rightarrow$ Fabrication
- Bringup, Qualification

Software Development

- Source Code (Java, C++)
- Assembly Language, Byte Code
- Binary Code
- Debugger
Defects

- Wafer size: 50mm – 500mm
- first test on wafer (mark defect parts with red dot)
- passing devices: cut out and put into package

packages:
- DIL
- quad-pack
- flip-chip
non-recurrent engineering (NRE) costs: $10M-$500M
mask set: $500k
die per chip: ~ $1
package: $2 - $10
effect of defects: cost ~ area^4
Normal Forms

- Full Adder
  - A
  - B
  - Cin
  - FA
  - S
  - Cout

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<th>Cin</th>
<th>Cout</th>
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Disjunctive Normal Form
- disjunction (OR) of minterms
- Implementation with NAND gates
- e.g. minterm: \((\neg A \land B \land Cin) \lor \ldots\)

Conjunctive Normal Form
- conjunction (AND) of maxterms
- implementation with NOR gates
- e.g. maxterm: \((\neg A \lor B \lor Cin) \land \ldots\)

siehe auch http://de.wikipedia.org/wiki/Konjunktive_Normalform
Design of Gates using Karnaugh Maps
• Logical Notation: \( z = \neg ((a \land b) \lor (c \land d)) \)

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<thead>
<tr>
<th>cd</th>
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\[ \text{Diagram:} \quad z = \neg a \lor \neg b \lor \neg c \lor \neg d \]
# Table of Logic Gates

<table>
<thead>
<tr>
<th>AND</th>
<th>OR</th>
<th>NOT</th>
<th>NAND</th>
<th>NOR</th>
<th>XOR</th>
<th>XNOR</th>
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<tbody>
<tr>
<td>ANSI (U.S.):</td>
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<td><img src="image5.png" alt="NOR" /></td>
<td><img src="image6.png" alt="XOR" /></td>
<td><img src="image7.png" alt="XNOR" /></td>
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<td>IEC (deutsch):</td>
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Multiplexer

- Selects one or another input based on control signal

<table>
<thead>
<tr>
<th>S</th>
<th>A</th>
<th>B</th>
<th>C</th>
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DNF (simplified):

\[ C = \neg S \land A \lor S \land B \]
DNF with NAND Gates
Adder Circuits

- **Half Adder**

  - **HA**

  - A → S
  - B → C

  - Truth Table:

    | A | B | C   | S   |
    |---|---|-----|-----|
    | 0 | 0 | 0   | 0   |
    | 0 | 1 | 0   | 1   |
    | 1 | 0 | 0   | 1   |
    | 1 | 1 | 1   | 0   |

- **Full Adder**

  - **FA**

  - A → S
  - B → Cout
  - Cin → Cout

  - Truth Table:

    | A | B | Cin | Cout | S   |
    |---|---|-----|------|-----|
    | 0 | 0 | 0   | 0    | 0   |
    | 0 | 0 | 1   | 0    | 1   |
    | 0 | 1 | 0   | 0    | 1   |
    | 0 | 1 | 1   | 1    | 0   |
    | 1 | 0 | 0   | 0    | 1   |
    | 1 | 0 | 1   | 1    | 0   |
    | 1 | 1 | 0   | 1    | 0   |
    | 1 | 1 | 1   | 1    | 1   |