Modern Computer Architecture

Lecture 1
Technical Background
• Introduction
• Silicon Technology
  – MOS FET: N-Switch and P-Switch
  – Logical Gates
  – Combinatorial Circuits
Semiconductors: Silicon

- most commonly: Si, but also GaAs, InP
- Symbol: Si, Atomic #14
- 2\textsuperscript{nd} most abundant element (after oxygen)
  27.7% mass of the earth crust,
  ➔ sand, glass
- diamond lattice
**n-type**
- Too many electrons in grid
- Travel faster

**p-type**
- Too few electrons in grid ("holes")
- Travel slower
Semiconductors: p-n junction

- p-n junction can be crossed by electric current only in one direction
- application: diode, LED
- Transistors can act as a switch for currents.
- Bipolar transistors are most commonly used in analog electronics.
- Disadvantage: requires current in steady state.  
  $\Rightarrow$ High power consumption.
MOSFET in action

Source     Gate     Drain
N+         depletion region
N+

P substrate

Source     Gate     Drain
Channel (Inversion layer)
N+         depletion region
N+

P substrate

voltage charge
- Logical Notation: \( y = \neg x \)
- Circuit Notation: \( y := \text{NOT} \ x \)

- if \( x=1 \): n-switch open, p-switch closed
- if \( x=0 \): n-switch closed, p-switch open

<table>
<thead>
<tr>
<th>( x )</th>
<th>( y )</th>
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- ANSI (U.S.):

- EIC (deutsch):

- DIN 40 700 (deutsch):
CMOS NAND Gate

- Logical Notation: $z = \neg (x \land y)$
- Circuit Notation: $z := \text{NOT} (x \text{ AND } y)$

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<tr>
<th>$x$</th>
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- ANSI (U.S.):

- EIC (deutsch):

- DIN 40 700 (deutsch):
p and n areas in CMOS form bipolar transistors
in normal operation, these transistors are not conducting
power surges or radiation can render these transistors in conducting state
effect: short-circuit, heat may lead to destruction of the device
Photolithography / Epitaxy

- physical vapor deposition (PVD)
- chemical vapor deposition (CVD)
- electrochemical deposition (ECD)
- molecular beam epitaxy (MBE)
- atomic layer deposition (ALD)

vapor-phase epitaxy (VPE)

expose

etch

glass
mask
acid
photoresist
new material
substrate
• At the bottom: MOS FETs from p- and n-doted silicon
• Short wires made from poly-silicon
• Several metal layers (up to 10) wires increase in width
Hardware Development

- Concept Engineering, Marketing
- Behavioral Modeling, Requirement Validation
- Architecture, Bit-Precise Modeling (e.g. in System-C)
- Testbench, Verification
- Silicon Frontend: RTL Modeling (e.g. Verilog, VHDL), clock-precise, Synthesis $\Rightarrow$ netlist
- Silicon Backend: Place&Route, Timing-/Power-Analysis $\Rightarrow$ geometry
- Tapeout $\Rightarrow$ Fabrication
- Bringup, Qualification

Software Development

- Source Code (Java, C++)
- Assembly Language, Byte Code
- Binary Code
- Debugger
Defects

- Wafer size: 50mm – 500mm
- first test on wafer (mark defect parts with red dot)
- passing devices: cut out and put into package

packages:
- DIL
- quad-pack
- flip-chip
Economics of Silicon Fabrication

- non-recurrent engineering (NRE) costs: $10M-$500M
- mask set: $500k
- die per chip: ~ $1
- package: $2 - $10

- effect of defects: cost ~ area^4
Normal Forms

- **Full Adder**

  ![Diagram of Full Adder]

  - Disjunctive Normal Form
    - disjunction (OR) of minterms
    - Implementation with NAND gates
    - e.g. minterm: \((\neg A \land B \land C_{in}) \lor \ldots\)

- **Conjunctive Normal Form**

  - conjunction (AND) of maxterms
  - implementation with NOR gates
  - e.g. maxterm: \((\neg A \lor B \lor C_{in}) \land \ldots\)

[Additional note: see also http://de.wikipedia.org/wiki/Konjunktive_Normalform]
- Logical Notation: \( z = \neg ((a \land b) \lor (c \land d)) \)
## Table of Logic Gates

<table>
<thead>
<tr>
<th></th>
<th>AND</th>
<th>OR</th>
<th>NOT</th>
<th>NAND</th>
<th>NOR</th>
<th>XOR</th>
<th>XNOR</th>
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<tbody>
<tr>
<td>ANSI (U.S.):</td>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
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<td>IEC (deutsch):</td>
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<td><img src="image13" alt="Diagram" /></td>
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<td>DIN 40 700 (deutsch, alt):</td>
<td><img src="image15" alt="Diagram" /></td>
<td><img src="image16" alt="Diagram" /></td>
<td><img src="image17" alt="Diagram" /></td>
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Multiplexer

- Selects one or another input based on control signal

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DNF (simplified):

\[ C = \neg S \land A \lor S \land B \]
DNF with NAND Gates
Adder Circuits

- **Half Adder**
  
  ![Half Adder Diagram]

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- **Full Adder**
  
  ![Full Adder Diagram]

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